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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/838,743	DEBOY ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

Amendment D filed 5/16/3 and entered as Paper No. 15 forms the basis of this Office Action. In Amendment D Applicant substantially amended claim 1 and added new claim 12. Claims 1 and 3-12 are in the application. For comments on Remarks by Applicant appended to said Amendment D please see "Response to Arguments" below.

Response to Arguments

1. Applicant's arguments filed 5/16/3 have been fully considered but they are not persuasive. Although Applicant's amendment of claim 1 removes the inconsistency of quantities of different dimensions equated to each other, except for a minor informality (see Objections to Claims), Applicant's claim still makes charge Q_c the sole criterion for avoiding breakdown, i.e., Q_c is defined as "the critical breakdown charge". As pointed out earlier, said "critical breakdown charge" must be translated or must be straightforwardly translatable, into maximally allowable field strength (see previous Office Action, page 3). Applicant has not provided said translation. Nor is it straightforwardly translatable into a maximally allowable field strength, as evidenced by the following example of a depleted (for simplicity here assumed to be) homogeneous layer of surface area F and thickness W: from integration of $\nabla . E = 4 \pi \rho$ it follows that the field strength E reached by fully depleting a homogeneous layer of thickness W and surface area $F >> W$ that has a charge density ρ as a result of said depletion is equal to $E = 4 \pi \rho W$, or, equivalently: $E = 4 \pi \rho_F W / F$, while Applicant's "critical breakdown

charge" Q_c, defined as "the charge quantity at which breakdown occurs" (cf. claims 1 and 12) is apparently introduced as a maximum value for ρ_F W, not as a maximum value for 4 π ρ_F W / F. The discrepancy defined by the presence of an extra factor 4 π / F is non-trivial, because F varies from device to device. No quantity F is even formally introduced. The invention thus as before must be characterized as not enabled by the specification.

Short of enablement, however, the examiner has not repeated the art rejections for claims 8-10 nor of claim 11, nor of newly added claim 12, because a reconsideration has cast reasonable doubt on the motivation and combinability of Park and Laska on the one hand and Yamaguchi for claims 8-10, and Yamamoto for claim 11.

Specification

No definition of critical surface charge associated with breakdown is complete without specifying at which surface said surface charge resides and in relation to which topography of conductors and other charges, because it is the local electric field that determines breakdown. In particular, given the said charge Q of the specification, the electric field is not determined at all. Instead, the surface area F over which the integration over dF is to be performed enters the relation between Q and E. Said surface area has not even been introduced. Furthermore, as a minor informality, throughout the specification the minus sign in the verbiage "∇. E = - 4 π ρ" (Gauss' law, or Poisson's law for electrostatic phenomena) needs to be omitted so as to replace said verbiage with "∇. E = 4 π ρ". Appropriate correction is required.

Claim Objections

2. ***Claims 1 and 12*** are objected to because of the following informalities:

the verbiage "in which ρ is the volume charge density" (line 33 of claim 1, line 35 of claim 12) should be changed to "in which ρ is the volume charge density and the integration over all surface area elements dF of said surface". Appropriate correction is required.

3. ***Claims 1 and 12*** are objected to because of the following informalities: the verbiage "∇. E = - 4 π ρ" should be "∇. E = 4 π ρ". Appropriate correction is required.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. ***Claims 1 and 3-12*** are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, with' regard to claim 1, line 32 and claim 12, line 34, particularly, the inequality involving inter alia the product of 0.9 and Q_c, the critical charge density Q_c is not linked to a maximum local electric field applied between said first and second electrode by Maxwell's equation. Poisson's equation merely connects the charge density to the local surplus of the electrostatic potential. This is not enough information, not for people of ordinary, - nor for those of extra-ordinary skills in the art, to determine Q_c. Nor does the mere knowledge of any Q_c constitute complete information about the maximum electric field strength. Because the purpose of the invention is avoidance of breakdown (see abstract and specification) the invention is not enabled.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. ***Claims 1 and 3-12*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular, the phrase "the critical breakdown surface charge denotes a critical value Q_c of the breakdown surface charge Q at which electrical breakdown is achieved" is indefinite, because Q is not related to the condition for electrical breakdown, i.e., for the condition of a local electric field exceeding the breakdown value.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. ***Claim 1*** is rejected under 35 U.S.C. 102(b) as being unpatentable over the conference publication by Laska et al (IEDM 90-807-810). Laska et al teach (cf. Figure 1) a vertically structured power semiconductor component, comprising:

a semiconductor body of first conductivity type (n type) and having a first main surface (upper main surface of n^- region) and a second main surface opposite said first main surface (bordering the lowest region marked "p");

a body zone (the highest region marked "p") of a second conductivity type (p type), i.e., opposite of said first conductivity type, introduced into said first main surface;

a zone (marked "n") of said first conductivity type (n type) disposed in said body zone;

a first electrode E making contact with said zone and with said body zone;

a second electrode disposed on said second main surface;

an insulating layer disposed on said first main surface (the insulating layer does feature on Figure 1, however is not explicitly indicated therein as such. However, the gate, to be discussed in the sequel is identified, while the device taught by Laska et al is a IGBT type device, i.e., insulated gate bipolar transistor; and hence the presence of said insulating layer between the gate and the substrate is inherent in the device);

a gate electrode G disposed above said body zone and separated from said body zone by said insulating layer; and an intersection of said semiconductor body and said body zone defining a pn junction (namely the common border between said semiconductor body and body zone), said semiconductor body having a layer thickness between said pn junction and said main surface selected such that when the maximum allowed blocking voltage or a voltage just less than said maximum allowed blocking voltage is applied between said first electrode and said second electrode, a space charge zone created in said semiconductor body meets said second main surface before a

field strength created by an applied blocking voltage reaches a critical value (cf. page 807, second column, from line 8 down).

Laska do not necessarily teach the specific charge density layer as mentioned in claim 1. However, it is obvious that breakdown needs to be avoided in any vertical power semiconductor component, while the margin to be observed, said margin here being evidently represented by the factor "0.9", is a matter of routine skills to those of ordinary skills in the art. Specifically, said factor "0.9" combined with the inequality as expressed in claim 1 is equivalent to the teaching of a range (0 – 0.9) in art in which the general conditions of the claim are met, in particular the condition to avoid undesirable breakdown. Applicant is reminded that it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

7. ***Claim 3*** is rejected under 35 U.S.C. 103(a) as being unpatentable over the conference publication by Laska et al (IEDM 90-807), in view of Hutchings et al (5,387,528). As detailed above, claim 1 (on which claim 3 depends) is unpatentable over Laska et al. Laska et al do not necessarily teach the further limitation defined by claim 3. However, it has long been standard in the art to dispose at the second main surface in IGFET devices a heavily doped semiconductor terminal regions of the same conductivity type as the substrate, as evidenced by Hutchings (heavily doped semiconductor terminal regions 4a (cf. column 6, lines 14-19), so as to mitigate the

large drop in conductivity between the electrode on said main second surface and the lowly doped semiconductor substrate 4. Because the purpose of Laska is to increase breakdown voltage of power IGFET devices whilst local gradients in the electrostatic potential determine whether a local breakdown condition is met, the motivation for the incorporation of the teachings in the above-described sense by Hutchings into the invention taught by Laska is evident. The inventions can be combined simply by replacement of the bottom part of the semiconductor body by a heavily doped semiconductor layer of the same type as said semiconductor body. Success in implementing the invention can thus be reasonably expected.

8. ***Claims 1 and 3-5*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Park (5,702,961) in view of the conference publication by Laska et al (IEDM 90-807-810).

With regard to claim 1: Park teaches (cf. Figure 1) a vertically structured power semiconductor component (cf. abstract, first sentence), comprising:

a semiconductor body of first conductivity type (n type) comprising subregions 104, 116 and 100 (cf. column 3, line 56, column 4, line 23, and column 6, line 45) and having a first main surface (upper main surface of the latter) and a second main surface opposite said first main surface (lower main surface of the latter);

a body zone 108 of a second conductivity type (p type), i.e., opposite of said first conductivity type, introduced into said first main surface (cf. column 4, lines 1-2);

a zone 110 of said first conductivity type (n type) disposed in said body zone (cf. column 4, lines 14-18);

a first electrode 114 making contact with said zone and with said body zone (cf. column 4, lines 27-28);

a second electrode 112 (cf. column 3, line 65) disposed on said second main surface;

an insulating layer disposed on said first main surface (the insulating layer does feature on Figure 1, however this is not explicitly indicated therein as such. However, the gate, to be discussed in the sequel is identified, while the device taught by Park is a IGBT type device, i.e., insulated gate bipolar transistor; and hence the presence of said insulating layer between the gate and the substrate is inherent in the device);

a gate electrode 118 (cf. column 4, line 19) disposed above said body zone and separated from said body zone by said insulating layer; and an intersection of said semiconductor body and said body zone defining a pn junction (namely the common border between said semiconductor body and body zone).

Park does not necessarily teach said semiconductor body to have a layer thickness between said pn junction and said main surface selected such that when the

maximum allowed blocking voltage or a voltage just less than said maximum allowed blocking voltage is applied between said first electrode and said second electrode, a space charge zone created in said semiconductor body meets said second main surface before a field strength created by an applied blocking voltage reaches a critical value. However, Laska et al, as discussed above, do teach this (cf. page 807, second column, from line 8 down) for the obvious reason to optimize thickness for improving the blocking voltage. Because blocking voltage improvement also is an objective of Park (see column 1, left column) there exists motivation to combine the references. Combination of the teachings by Park and Laska et al is possible, because all that is needed is an appropriate selection for the thickness of the semiconductor body. Expectation of success in combining the references is reasonable, considering the independence of said thickness of all other limitations in claim 1.

With regard to claim 3: the semiconductor body taught by Park has heavily doped terminal regions 100 of first conductivity type (n-type) disposed at said second main surface.

With regard to claim 4: Park teaches the preferential inclusion of a further zone 116 of said first conductivity type disposed in the vicinity of said second main surface (cf. column 3, line 53).

With regard to claim 5: Park teaches punch-through regions disposed between said heavily doped terminal regions (cf. regions 102-100-102-100 alternating in doping type). The statement in claim 5 on current control is inherent in the device limitation stated up to this point in the claim.

9. ***Claim 6*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Park and Laska et al (IEDM 90-807-810) as applied to claim 1 above, and further in view of Fruth et al (6,011,280), or, -in the alternative, as being unpatentable over Laska et al (IEDM 90-807-810) in view of Fruth et al (6,011,280). As detailed above, Laska et al anticipate claim 1, while claim 1 also is unpatentable over Park in view of Laska et al. Neither Laska et al nor Park necessarily teach the further limitation defined by claim 6. However, the application of (a) edge termination 34/30 and a (b) channel stop 40 to mitigate the effect of geometrically enhanced edge electric fields through screening provided by dopants and for the purpose of termination the device region, respectively, is well known in the art, as witnessed by Fruth et al (see column 1, line 56 – column 2, line 16).

10. ***Claim 7*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Park, Laska et al and Fruth as applied to claim 6 above, and further in view of Feiler (6,236,068 B1). As detailed above, claim 6 (on which claim 7 depends) is unpatentable over Park, Laska et al and Fruth, or, in the alternative, over Laska et al and Fruth, none of whom necessarily teach the further limitation as defined by claim 7. However, as witnessed by Feiler (cf. Figure 3 and column 6, lines 2-6) it would have been obvious to one of ordinary skill in the art of MOS technology to include the further limitation of claim 7 because source magnetoresistors are thus used to reduce electric field peaks, for example in the vicinity of the gate electrode.

The work by Laska et al aims to prevent punch-through (cf. title and abstract). Breakdown is equally a concern in Park (cf. column 3, lines 5-8). In conclusion, there is ample *motivation* to combine the teaching in this regard by Feiler with Laska et al and, in the alternative, with Park and Laska et al. *Combination* of the teaching by Feiler with the inventions by Laska et al, and, in the alternative, with the invention by Park and Laska et al, is straightforward: the inclusion of a source magneto-resistor can be achieved in a modular fashion, because said magneto-resistor is an additional and modular component extraneous to the substrate. *Success* in implementing the combination can therefore be reasonable expected.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
July 21, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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